

DRAM BIT LINES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to the manufacturing of DRAM devices. More specifically, the present invention relates to the forming of bit line structures in such memories.

Description of the Related Art

Fig. 1 partially and schematically illustrates in a top view, and Figs. 2A, 2B, 2C in a cross-section view along respective axes A-A, B-B, and C-C, the structure of an elementary cell 1 of a DRAM of folded bit line type under manufacturing in a semiconductor substrate 2, typically single-crystal silicon. A memory includes a plurality of such identical elementary cells 1 arranged in rows and columns. Each elementary cell 1 is formed in an active region 3, generally rectangular, delimited in substrate 2 by insulating trenches 4. Insulating trenches 4 are obtained by digging into substrate 2, then filling the formed hollowings with an insulating material, generally silicon oxide (SiO_2). In Fig. 1, the limit between active region 3 and insulating trenches 4 is illustrated by stripe-dot lines.

Four conductive lines WL1, WL2, WL3, and WL4 cross the cell. Each of these lines, which are the word lines of the general memory device, is insulated from the underlying active areas 3 by an insulating layer 7, typically silicon oxide. Their lateral walls are conventionally provided with spacers 8. Two "active" word lines WL2 and WL3 cross the cell in its active region 3. Active word lines WL2 and WL3 are common to all cells of a same row. The other two word lines WL1 and WL4 run over either side of active region 3, that is, over insulating trenches 4. Each of word lines WL1 and WL4 is one of the two active word lines of two different elementary cell rows, these two rows (not shown) being distinct from that containing elementary cell 1.

After formation of word lines WL1, WL2, WL3, and WL4, heavily-doped regions 9 and 10 of a conductivity type opposite to that of substrate 2 have been formed by implantation/diffusion at the surface of active region 3.

Active word lines WL2, WL3 then form the gates of two MOS transistors of the same type, having common drain/source regions 9 and distinct source/drain regions 10, each formed in the active region 3 between spacer 8 of the corresponding word line and the neighboring insulating trench 4.

Substrate 2 (active region 3 and trenches 4) and lines WL1, WL2, WL3, and WL4 are altogether covered with a thick insulating layer 11, typically silicon oxide. The upper surface of layer 11 is substantially planar. Layer 11 has been locally opened to at least partially expose the three semiconductor regions 9 and 10. Contacts 5 and 6, respectively with drain/source region 9 and each of source/drain regions 10, result from the filling of the openings thus formed by means of a conductive material, typically metal, generally tungsten.

A bit line BL, common to the cells of a same column, runs over layer 11 above an insulating trench 4 separating two distinct cell columns. Bit line BL is encapsulated by an insulating structure 12. Bit line BL is designed to contact drain/source region 9 via contact 5.

Bit line BL may be formed before or after two memory points (capacitors) not shown, also formed on layer 11, but each in contact with one of the two source/drain regions 10 via a contact 6.

Be they formed after or before bit lines BL, the memory point structures must then take into account the presence or the subsequent forming thereof on a same level (the upper surface of layer 11). This leads to managing manufacturing constraints, in particular alignment constraints, which complicate processes.

More specifically, protecting the structure against possible capacitive couplings or short-circuits, caused by misalignments of masks of formation of bit lines or memory points, limits the density of the obtained memory device.

Further, since the planar surface area available on layer 11 is limited, obtaining memory devices with capacitors having a sufficient capacitance imposes using memory points with a complex structure and/or limiting the device density.

SUMMARY OF THE INVENTION

5 An embodiment of the present invention provides a novel manufacturing method of a DRAM device, which reduces the preceding constraints.

The method is compatible with the forming of the DRAM on a same substrate as a logic circuit external to the memory.

10 The method includes two active word lines having a common drain/source region and having distinct source/drain regions contacting two memory points, including, after the forming of insulated conductive lines, the steps of:

a) depositing a first insulating layer;

b) depositing a second insulating layer, selectively etchable with respect to the first insulating layer;

15 c) etching the second insulating layer to only maintain it above the insulated conductive lines, at least inside and around an active region;

d) depositing and leveling a third thick insulating layer selectively etchable with respect to at least the second insulating layer;

20 e) opening the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench;

f) depositing a conductive material to fill the previously-formed opening;

g) performing a chem-mech polishing of the entire structure; and

h) depositing a fourth insulating layer, selectively etchable with respect to the third insulating layer.

25 According to an embodiment of the present invention, step e) consisting of opening the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench is implemented to open the first and third

insulating layers to at least also partially expose the source/drain regions, the conductive material deposited at step f) being deposited to fill all the openings thus formed.

According to an embodiment of the present invention, step e) consisting of opening the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench is preceded by the steps of:

i) opening the first and third insulating layers to at least partially expose the source/drain regions;

j) depositing a conductive material in the openings thus formed; and

k) performing a chem-mech polishing of the entire structure, whereby contacts are formed with the source/drain regions.

According to an embodiment of the present invention, step k) of chem-mech polishing is followed by the deposition of an additional insulating layer on the entire structure, step e) then consisting of successively opening the additional insulating layer and the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench.

According to an embodiment of the present invention, step g) of chem-mech polishing of the entire structure, or step h) of deposition of the fourth insulating layer, selectively etchable with respect to the third insulating layer, is followed by the steps of:

l) opening the first and third insulating layers to at least partially expose the source/drain regions;

m) depositing a conductive material in the openings thus formed; and

n) performing a chem-mech polishing of the entire structure, whereby contacts are formed with the source/drain regions.

According to an embodiment of the present invention, step a) of deposition of the first insulating layer is preceded by the deposition of an additional insulating layer selectively etchable with respect to the filling material of underlying insulating trenches and with respect to the first insulating layer.

According to an embodiment of the present invention, the first and third insulating layers are made of silicon oxide (SiO_2) and the second and fourth insulating layers as well as the additional insulating layer are made of silicon nitride (Si_3N_4).

5 According to an embodiment of the present invention, the memory cell is formed in a same substrate as logic circuits.

The present invention also provides a DRAM cell structure including two inactive word lines formed on insulating trenches, on either side of an active region of a substrate, and two active word lines having a common drain/source region and having distinct source/drain regions contacting two memory points, the four word lines, the
10 insulating trenches, and the substrate being covered at least partially with a multiple-layer of at least three insulating layers, formed of first and third layers deposited over the entire structure, and of a second layer removed from the active region, except above the word lines, and being made of a material selectively etchable with respect to the first and third layers, and a bit line of the cell directly resting upon at least a portion of its drain/source
15 region as well as on a neighboring insulating trench, the bit line and the third insulating layer being covered with a fourth insulating layer selectively etchable with respect to the third layer.

According to an embodiment of the present invention, the multiple-layer rests upon an additional insulating layer selectively etchable with respect to the first
20 superposed insulating layer and with respect to the filling material of the underlying insulating trenches.

The foregoing objects, features and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

25 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 schematically illustrates, in top view, an elementary cell of a DRAM plane at an intermediary stage of its forming;

Figs. 2A, 2B, and 2C show, in partial and simplified cross-section views, the elementary cell of Fig. 1 formed according to state-of-the-art methods;

5 Figs. 3A, 3B, 3C, and 3D show, in partial and simplified cross-section views, an elementary cell at different steps of its manufacturing according to the present invention;

Fig. 4 shows, in a cross-section view along axis B-B, the elementary cell of Fig. 1 formed according to the present invention; and

Fig. 5 shows, in a cross-section view along axis C-C, the elementary cell of Fig. 1 formed according to the present invention.

10 DETAILED DESCRIPTION OF THE INVENTION

For clarity, the same elements have been referred to with the same references in the different drawings and, further, as usual in the representation of integrated circuits, the different cross-section views are not drawn to scale.

15 An embodiment of the present invention will be illustrated hereafter in relation with Figs. 3A to 3D applied to the forming in a same substrate of CMOS-type logic circuits and of an elementary cell of a DRAM device of folded bit line type. More specifically, the logic side has been shown to the left of Figs. 3A to 3D and the memory side has been shown to the right.

20 It is desired to form an elementary cell having a structure in top view identical to that illustrated in Fig. 1. Figs. 3A to 3D show, on the right-hand side, elementary cell 1 of Fig. 1 in cross-section along its main orientation axis, that is, line A-A of Fig. 1.

Fig. 3A illustrates the result of initial steps of a method according to the present invention. On the logic side and on the memory side, active areas 3 have first been
25 defined in a single-crystal silicon substrate 2, for example, by forming insulating trenches 4 filled with an insulating material, for example, silicon oxide. Then, a thin dielectric layer 7 and a conductive layer 13 have been successively formed and etched to define, on the memory and logic sides, insulated conductive structures. More specifically, on the

memory side, these structures cross the entire memory plane to form word lines of the memory array. Elementary cell 1 is crossed in its active portion by two word lines WL2 and WL3, and surrounded by two word lines WL1 and WL4 running above insulating trenches 4.

5 On the memory and logic side, the lateral walls of the different insulated conductive structures thus formed are covered with insulating spacers 8.

An implantation/diffusion of a dopant of a conductivity type opposite to that of substrate 2 has then been performed to form, on the logic side and on the memory side, in active areas 3, MOS transistor sources and drains.

10 On the memory side, active word lines WL2 and WL3 form the gates of two such transistors and define, in underlying active area 3, a channel region separating drain/source regions 9 and source/drain regions 10. More specifically, source/drain regions 10 of the two resulting MOS transistors are distinct and formed between the gate structures and insulating trenches 4. However, their drain/source region 9 is common, and formed
15 between lines WL2 and WL3.

On the logic side, the insulated conductive structure 7 also forms the gates of MOS transistors and define a channel region separating drain/source and source/drain regions 109 and 110.

Three insulating layers 14, 15, and 16 are then successively deposited. The
20 first insulating layer 14 is made of a material selectively etchable with respect to substrate 2 and to the material filling underlying insulating trenches 4. Layer 15 is made of an insulating material selectively etchable with respect to underlying layer 14. Finally, layer 16 is made of an insulating material selectively etchable with respect to underlying insulating layer 15. The nature of layer 16 will be specified hereafter, in relation with Fig.
25 3B.

At the next steps, illustrated in Fig. 3B, insulating layer 16 is removed on the logic side. On the memory side, insulating layer 16 is etched to be maintained and to extend slightly beyond word lines WL1, WL2, WL3, and WL4. This etching is followed by the deposition of a thick insulating layer 11. Layer 11 is made of a material selectively

etchable with respect to the insulating material of the remaining portions of layer 16. In accordance with standard CMOS methods implemented on the logic side, it is preferable for thick insulating layer 11 to be made of silicon oxide. Insulating layer 16 will then be made of an insulating material other than silicon oxide. It may however be of same nature as layer 14, for example, silicon nitride (Si_3N_4). Layer 15 may however be of same nature as layer 11.

At the next steps, illustrated in Fig. 3C, openings are formed in layer 11. On the logic side, these openings are formed to expose either semiconductive regions of substrate 2, for example, source/drain regions 110 and/or drain/source regions 109 of the logic transistors, or conductive lines 13 forming the gate electrode of the logic transistors, or to simultaneously expose some of these regions. On the memory side, the common drain/source region 9 is at least partially exposed between active word lines WL2, WL3.

For this purpose, as illustrated in Fig. 3C, layers 11, 15, and 14 are successively etched on the memory side and on the logic side. Assuming that layers 11 and 15 are of same nature, they are etched simultaneously. In case of a misalignment of the mask upon etching of insulating layers 11 and 15, on the memory side, the portions of layer 16 above the word lines remain intact, as illustrated above line WL2. Indeed, layers 11 and 15 on the one hand and layer 16 on the other hand, are made of materials selectively etchable with respect to each other.

According to an embodiment, on the memory side, layers 11, 15, and 14 are first opened to expose source/drain regions 10. The openings thus formed are then filled with a conductive material to form contacts 6. The conductive structures of neighboring word lines WL1, WL2, WL3, and WL4 are then protected, as will be further detailed hereafter, against a possible misalignment of the opening mask of layer 11 by the remaining portions of insulating layer 16.

Then, on the memory side and on the logic side, layers 11 and 15 are etched above drain/source regions 9, and the insulating layer of different nature 14 is etched. At this stage of the process, on the memory side, the possibly exposed portions of layer 16

may be etched if layer 16 is of the same nature as layer 14, but the etching will then stop at the level of layer 15, which is of a different nature.

A conductive material 18 is then deposited and etched. Preferably, conductive material 18 is a metal, for example, tungsten. Material 18 is then etched to be removed from the upper horizontal planar surfaces of thick insulating layer 11. This removal may advantageously be performed by a chem-mech polishing method (CMP).

On the memory side, the etching of insulating layers 11, 16, 15, and 14 has been performed so that the opening thus formed extends, as better illustrated in Fig. 5, above active region 3 and an insulating trench 4 separating two cell columns. This extension is formed in a perpendicular plane to be continuous in the entire memory plane, as better illustrated in Fig. 4, which shows a cross sectional view along axis B-B of Fig. 1. Thus, upon deposition of conductive material 18, a bit line BL is formed in this extension. Bit line BL is then directly put in contact with region 9, between two memory cell columns.

On the logic side, it should be noted that material 18 enables transferring to an upper level a contact with an underlying semiconductor region 109, and/or putting in electric contact different portions of the logic circuit, such as, for example, source/drain region 110 and gate 13 of a logic transistor.

At the next steps, illustrated in Fig. 3D, an insulating layer 19 is deposited on the planar surface of layer 11 and of the openings filled with material 18. Insulating layer 19 is made of a material selectively etchable with respect to underlying insulating layer 11 and with respect to conductive material 18. It should be noted that layer 19 is deposited to maintain the planarity of the structure.

Layer 19 is etched to be suppressed on the memory side above contacts 6 formed with source/drain semiconductor regions 10. On the logic side, layer 19 may be completely removed, as illustrated, or only removed at the locations where contacts must subsequently be formed. It may also be maintained in place to be used as an etch stop and/or protective coating layer in case of a misalignment of a mask in a subsequent etching.

Then, the process carries on to form memory points (capacitors) in contact with underlying semiconductor regions 10 via contacts 6.

At this stage of the process, the problems linked to the subsequent/previous forming of bit lines above thick insulating layer 11 are advantageously avoided. This enables increasing the density of the formed memory device, while being compatible with standard CMOS process sequences. Further, since the surface of layer 19 on which the memory points (capacitors) are formed is planar, and not deformed by protruding bit line structures, the memory point forming will be simplified.

Figs. 4 and 5 illustrate, in respective cross-section views along lines B-B and C-C of Fig. 1, the state of elementary cell 1 of Fig. 1, formed according to the present invention. More specifically, elementary cell 1 is shown at the manufacturing step of Fig. 3D.

Fig. 4 illustrates a portion of substrate 2 having its surface entirely formed of an insulating trench 4 separating two memory cell columns. The four word lines WL1, WL2, WL3, and WL4 run over trench 4. The word lines are covered with insulating layers 14, 15 and 16. All of this is covered with conductive material 18 and insulating layer 19. The resulting bit line BL thus crosses the different word lines WL1, WL2, WL3, and WL4 without reaching them. Further, bit line BL is protected from the memory point structures subsequently formed by superposed insulating layer 19.

Fig. 5 illustrates the width of cell 1. Active region 3, the surface of which is formed of the sole drain/source region 9 common to the two active word lines of cell 1, is defined in substrate 2 by insulating trenches 4. A multiple-layer of insulating layers 14, 15, 16, and 11 is cut by a conductive column 18 at least partially in contact with region 9 and extending laterally above an insulating trench 4. Conductive column 18 forms bit line BL interconnecting drain/source regions 9 of all the cells in a same column.

According to a specific embodiment of the present invention, the nature and thickness of the different layers are the following:

- gate insulator 7: silicon oxide, from 1 to 10 nm, for example, 3 nm;
- gate conductor 13: polysilicon;
- spacers 8: silicon nitride;
- insulating layer 14: silicon nitride, from 10 to 300 nm, for example, 80 nm;

- insulating layer 15: silicon oxide, from 10 to 300 nm, for example, 80 nm;
- insulating layer 16: silicon nitride, from 10 to 300 nm, for example, 80 nm;
- insulating layer 11: silicon oxide, from 100 to 800 nm, for example, 500 nm; and

- 5 - insulating layer 19: silicon nitride, from 10 to 300 nm, for example 80 nm.

Further, the materials of bit line BL and of contacts 6 may be of same nature, preferably metal, for example, tungsten. However, it will be possible to use conductor or semiconductor materials, and/or to use different materials.

10 In the case where bit lines BL and contacts 6 are made of a same material, they may be formed simultaneously, instead of being formed successively as previously discussed in relation with Fig. 3C.

15 In the case where bit lines BL and contacts 6 are made of different conductive materials, if these materials are selectively etchable with respect to each other, contacts 6 may be formed, as discussed previously in relation with Fig. 3C, before bit lines BL. However, contacts 6 may also be formed after the forming of bit lines BL. If the materials forming bit lines BL and contacts 6 are selectively etchable with respect to each other, contacts 6 may then indifferently be formed before or after deposition and etching of layer 19.

20 If the materials forming bit lines BL and contacts 6 are different from each other, contacts 6 may further be formed before or after bit lines BL. However, if they are formed before the bit lines, the additional deposition of a protective insulating layer will be provided. This layer will then preferably be of same nature as underlying thick insulating layer 11. It will be, considering the previously-detailed example of embodiment, a silicon oxide layer having a thickness ranging between 10 and 300 nm, for example 80 nm.

25 However, if contacts 6 are formed after bit lines BL, they will preferably be formed after the deposition and etching of layer 19, to protect bit lines BL upon etching of the material forming contacts 6.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In

particular, it applies to any process of simultaneous manufacturing of MOS transistors and of DRAM cells incorporating steps of a standard CMOS process. Thus, the nature and thickness of each of the layers may be modified according to the constraints linked to the standard CMOS processes in which the steps specific to the memory cell forming are incorporated. Thus, the insulators used to form layers 14, 15, and 16 may be chosen from among the various known materials or combinations thereof, for example, in the form of multiple-layers. It will however be ascertained in this latter case to respect the previously-discussed constraints of protection of the word lines against misalignments upon opening of contacts towards underlying semiconductor regions.

Further, although the use of a first insulating layer 14 selectively etchable with respect to the insulating material of trenches 4 and of upper layer 15 is preferred, it is possible to only use the combination of layers 15 and 16 to ensure the protection of the word lines against the bit lines. The function of layer 14 only is to avoid an overetching of insulating trench 4 when said trench is formed of an insulating material of same nature as upper insulating layer 15.

Moreover, the deposition of any metal conductive layer may be preceded by the deposition of a bonding and/or etch stop layer.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.